What is claimed is:

1. A computer system, unaffected by memory module instability, comprising:

at least one memory mirror unit controlling a plurality of memory modules and receiving an error control signal, wherein each of the memory mirror units writes data to the corresponding memory modules during a write cycle and activates a first memory module among the memory modules, reading data during a read cycle;

a memory controller enabling the error control signal upon detection of a read error in the first memory module, wherein the memory mirror unit disables the first memory module and activates a second memory module among the memory modules when the read error occurs in the first memory module.

2. The computer system as claimed in claim 1, further comprising:

a central processing unit (CPU); and

a system interruption device providing an interruption signal to the CPU to interrupt system operations and then activate the corresponding error control signal when the memory controller detects the read error.

3. The computer system as claimed in claim 2, wherein each memory mirror unit receives a corresponding

error control signal for control of corresponding memory modules.

4. The computer system as claimed in claim 3, wherein the memory controller determines that the read error has occurred when the memory controller detects an irreparable error in the first memory module of corresponding memory modules during the read cycle.

5. The computer system as claimed in claim 3, wherein the memory controller determines that the read error has occurred when the memory controller detects that the number of errors in the first memory module reaches a predetermined value.

6. The computer system as claimed in claim 3, wherein each memory mirror unit controls only a first and second memory module, each memory mirror unit activating the first and second memory modules during the write cycle and only activating the first memory module during the read cycle, and wherein the memory controller activates the error control signal and the memory mirror unit only activates the second memory module upon detection of the read error in the first memory module during the read cycle.

7. The computer system as claimed in claim 3, wherein each memory mirror unit comprises:

a first AND gate comprising a first input terminal, a second input terminal, a third input terminal receiving a row selecting signal, a fourth input terminal, a fifth input terminal

receiving a write enable signal, and a sixth input terminal receiving the error control signal;

a first inverter comprising an input terminal receiving a chip control signal and an output terminal coupled to the first input terminal of the first AND gate;

a second inverter comprising an input terminal receiving a first enable signal and an output terminal coupled to the second input terminal of the first AND gate;

a third inverter comprising an input terminal receiving a column selecting signal and having an output terminal coupled to the fourth input terminal of the first AND gate;

a second AND gate comprising a first input terminal, a second input terminal, a third input terminal receiving the row selecting signal, a fourth input terminal, a fifth input terminal receiving the write enable signal, and a sixth input terminal;

a fourth inverter comprising an input terminal receiving the chip control signal and an output terminal coupled to the first input terminal of the second AND gate;

a fifth inverter comprising an input terminal receiving a second enable signal and an output terminal coupled to the second input terminal of the second AND gate;

a sixth inverter comprising an input terminal receiving the column selecting signal and an output terminal coupled to the fourth input terminal of the second AND gate;

a seventh inverter comprising an input terminal receiving the error control signal and an output terminal coupled to the sixth input terminal of the second AND gate;

a first switch comprising an output terminal, a control terminal, and an input terminal receiving the first enable signal;

a second switch comprising an input terminal receiving the second enable signal, an output terminal coupled to the output terminal of the first switch and a control terminal receiving the chip enable signal;

an eighth inverter comprising an input terminal receiving the chip enable signal and an output terminal coupled to the control terminal of the first switch;

a first OR gate comprising a first input terminal receiving the first enable signal, a second input terminal coupled to the output terminal of the first AND gate, and an output terminal coupled to the first memory module; and

a second OR gate having a first input terminal coupled to the output terminal of the first switch, a second input terminal coupled to the output terminal of the second AND gate, and an

output terminal coupled to the second memory module.

8. The computer system as claimed in claim 7, wherein the chip control signal equalizes the addresses of the first and second memory modules.

9. The computer system as claimed in claim 7, wherein the memory controller determines that a read error has occurred when the memory controller detects an irreparable error in the first memory module during the read cycle.

10. The computer system as claimed in claim 8, wherein the memory controller determines that a read error has occurred when the memory controller detects the number of errors in the first memory module during the read cycle reaching a predetermined value.

11. The computer system as claimed in claim 9, wherein the chip control signal and the error control signals are output from a general input/output device of the computer system and wherein the first enable signal, the second enable signal, the row selecting signal, and the column selecting signal are output from the memory controller.

12. The computer system as claimed in claim 9, wherein the chip control signal is output from a general input/output device of the computer system and wherein the error control signal, the first enable signal, the second enable signal, the row selecting signal, and the

column selecting signal are output from the memory controller.

13. The computer system as claimed in claim 10, wherein the error control signal is output from a general input/output device of the computer system and wherein the first enable signal, the second enable signal, the row selecting signal, and the column selecting signal are output from the memory controller.

14. The computer system as claimed in claim 10, wherein the chip control signal is output from a represent general input/output device of the computer system and wherein the error control signal, the first enable signal, the second enable signal, the row selecting signal, and the column selecting signal are output from the memory controller.

15. A method for controlling memory of a computer system, the method comprising the steps of:

providing at least one memory mirror unit, each controlling a memory module group having a plurality of memory modules;

equalizing addresses of the memory modules inside each memory module group;

writing data to the corresponding memory modules according to a write address during a write cycle; and

reading a first memory module according to a read address during a read cycle;

wherein the computer system activates an error control signal received by the corresponding memory mirror unit to select a second memory module from corresponding memory modules when a read error occurs in the first memory module.

16. The method as claimed in claim 15, wherein the computer system determines that the read error has occurred when an irreparable error occurs in the first memory module of the corresponding memory modules.

17. The method as claimed in Claim 15, wherein the computer system determines that the read error has occurred when the number of errors in the first memory module reaching a predetermined value.

18. A method for controlling memory of a computer system, the method comprising the steps of:

providing at least one the memory mirror unit each controlling a first and second memory module;

equalizing addresses of the first and second memory modules;

writing data to first and second memory modules according to a write address during a write cycle; and

reading the corresponding first memory module according to a read address reading data during a read cycle;

wherein the computer system activates an error control signal received by the corresponding

memory mirror unit to select a corresponding second memory module when a read error in the corresponding first memory module is detected.

19. The method as claimed in claim 18, wherein the computer system determines that the read error has occurred when an irreparable error occurs in the first memory module during the read cycle.

20. The method as claimed in Claim 18, wherein the computer system determines that the read error has occurred when the number of errors in the first memory module reaches a predetermined value.